EUROPEAN PATENT APPLICATION

(54) Charge-coupled device.

(57) A charge-coupled device having a semiconductor body (1) comprising a semiconductor layer (3) of a first conductivity type adjoining a surface (2), means for depleting the semiconductor layer (3) throughout its thickness whilst avoiding breakdown, a sequence of transport electrodes (6, 7, 8) on the surface (2) above the semiconductor layer (3), which are separated by a blocking layer (9) from this layer and are connected to the clock voltage sources (10) to form in the semiconductor layer (3) of the surface (2) mutually separated potential wells for storing and transporting information-carrying charge packets. The device further comprises an input stage (I) having a supply zone (11) for supplying said majority charge carriers and an input electrode (13), which is located between the supply zone (11) and the transport electrodes (6, 7, 8) and is separated by an isolating layer (9) from the semiconductor surface (2), an input signal source (15) and means for forming under the input electrode (13) a potential well whose minimum is located closer to the surface (2) than to the transport electrodes (6, 7, 8).

According to the invention, a dopant of the second opposite conductivity type is introduced between the supply zone (11) and the transport electrodes (6, 7, 8) in such a manner that the net doping of the first conductivity type in the part (I) of the semiconductor layer (3) between the supply zone (11) and the transport electrodes (6, 7, 8) is lower than in the remaining part of the layer.

Preferably, the width of the electrodes of the input stage (I) is chosen so that the transport capacity of these electrodes is practically equal to that of the transport electrodes (6, 7, 8).
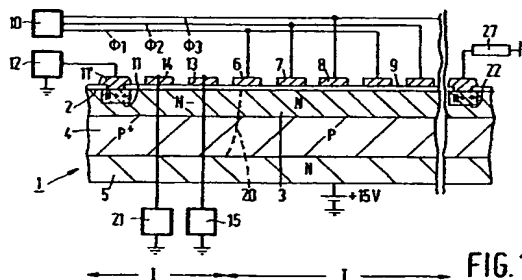
FIG. 1

CHARGE-COUPLED DEVICE.

The invention relates to a charge-coupled device having a semiconductor body comprising a semiconductor layer of a first conductivity type adjoining a surface, means for depleting the semiconductor layer throughout its thickness at least in the absence of supply of majority charge carriers whilst avoiding breakdown, a sequence of transport electrodes on the surface above the semiconductor layer, which are separated from this layer by a blocking layer and are connected to clock voltage sources to form in the semiconductor layer potential wells separated from the surface for storing and transporting information-carrying charge packets, an input stage comprising a supply zone for supplying said majority charge carriers and an input electrode, which is located between the supply zone and the transport electrodes, is separated from the semiconductor surface by an isolating layer and by which in the semiconductor layer a potential well can be induced with an input signal source for applying a voltage difference between the supply zone and the input electrode, which determines the value of a charge carrier packet flowing from the supply zone into the potential well under the input electrode, while in order to obtain a practically linear relation between the value of the said charge carrier packet and the input signal means are provided by which a potential well can be obtained under the input electrode whose minimum is located closer to the surface than in the potential wells induced under the transport electrodes.

Such a charge-coupled device is known from

Charge-coupled devices with charge transport at a certain distance from the surface, so-called bulk transport, are well known and are designated by the abbreviations BCCD ("Buried Channel Charge-Coupled Device") and PCCD ("Peristaltic Charge-Coupled Device"). They are distinguished from analogue devices in which the charge transport takes place along the surface inter alia in that the transport efficiency is substantially not influenced by surface states. Moreover, in this device, the charge transport takes place under the influence of comparatively strong electrical fields because of the comparatively large distance between the charge packets and the transport electrodes. Devices of the BCCD type therefore generally operate at a very high speed.

It is desirable for most applications that the value of the charge packet to be formed under the input electrode varies practically linearly with the value of the input signal given at the input electrode.

In charge-coupled devices of the BCCD type,

however, potential wells are formed whose minimum is located at a certain distance from the semiconductor surface. With increasing value of the introduced charge packet, the stored charge always lies closer to the surface. The capacity of the charge storage space is therefore not constant, but increases with the value of the charge packet, so that upon conversion of the input signal into a charge packet a non-linearity is introduced. Therefore, attempts have been made to eliminate this undesired non-linearity in the input characteristic of such charge-coupled devices. For this purpose, it is suggested in the aforementioned US-A-4280068 to generate under the input electrode a potential well whose minimum is located at a smaller distance from the surface than the minima of the potential wells generated under the transport electrodes. Due to the fact that it has been found that comparatively large quantities of charge can be stored closer to the surface without large capacity variations, in this manner a more linear input characteristic is obtained.

However, it has been found that also with the use of this measure in many cases the linearity of the input characteristic is nevertheless insufficient.

The invention has inter alia for its object to eliminate entirely or practically entirely the remaining non-linearity of the input characteristic in a charge-coupled device of the kind described.

The invention is based inter alia on the recognition of the fact that it is possible that by means of an additional doping or implantation step the input capacitance is determined practically entirely by the (linear) capacitance of the isolating layer under the input electrode.

According to the invention, a charge-coupled device of the kind described in the opening paragraph is characterized in that a dopant of the second opposite conductivity type is introduced between the supply zone and the transport electrodes in such a manner that the net doping of the first conductivity type in the part of the semiconductor layer between the supply zone and the transport electrodes is lower than in the remaining part of the layer.

The input characteristic of a charge-coupled device according to the invention has a strongly improved linearity. This is due to the lower net doping of the semiconductor layer under the input electrode. The charge packet introduced via this electrode is taken up for the major part by the capacitance formed by the isolating layer. However, a small part of the charge is taken up by the part of the semiconductor layer located under the input electrode.

This remaining charge part, which causes the non-linearity, is reduced considerably in the charge-coupled device according to the invention due to the reduced net doping of said semiconductor region so that the input capacitance is determined practically entirely by the linear capacitance of the isolating layer.

Since the input stage is designed to operate in the accumulation mode, that is to say that the induced charge is stored at least for an important part near the surface, the charge transport capacity per unit of electrode width will be larger than at the transport electrodes. Therefore, the width of the electrodes of the input stage is therefore chosen so that the transport capacity of these electrodes is practically equal to that of the transport electrodes. Advantageously, the net doping of the semiconductor layer under the input electrode is chosen so that in the operating condition due to the difference in threshold voltage between the input electrode and the transport electrodes an additional electrical field is obtained in the transport direction.

In many cases, a sampling electrode is provided advantageously between the supply zone and the input electrode for sampling the input signal, this sampling electrode being provided with means by which during sampling a potential can be applied in the semiconductor layer, by which the supply of majority charge carriers from the supply zone to the input electrode can be blocked.

The invention will now be described more fully with reference to an embodiment and the drawing, in which:

Fig. 1 shows diagrammatically in cross-section a charge-coupled device according to the invention,

Fig. 2 shows diagrammatically in plan view a part of the electrode structure of the device shown in Fig. 1, and

Fig. 3 shows the variation with time of the clock voltages to be applied to the electrodes.

The Figures are purely schematic and not drawn to scale, while for the sake of clarity especially the dimensions in the direction of thickness are exaggerated. In the cross-sections, semiconductor regions of the same conductivity type are generally cross-hatched in the same direction. Corresponding parts are generally designated in the different Figures by the same reference numerals.

Fig. 1 shows diagrammatically in cross-section an embodiment of a charge-coupled device according to the invention. The device according to this embodiment is intended to be used for image transport, but the invention may also be used in other charge-coupled devices. The device comprises a semiconductor body 1 made in this embodiment of silicon and having a semiconductor layer 3 of the first conductivity type, which adjoins

a surface 2 and in which the charge transport takes place.

In this embodiment, the layer 3 consists of n-type silicon. The thickness and the doping concentration of the layer 3 are so small that the layer 3 - at least in the absence of the supply of majority charge carriers - can be depleted throughout its thickness without breakdown occurring. The layer 3 is formed in this embodiment by an implantation of phosphorus ions at a dose of $1.18 \cdot 10^{12}$ ions/cm^2 and at an energy of 100 keV. The layer 3 has a thickness of 1.08 μm and is bounded in this embodiment on its lower side by a p-type layer 4, which forms a p-n junction with the layer 3. The layer 4 is formed by an implantation of boron ions down to a depth of 3.8 μm at a dose of $9.0 \cdot 10^{11}$ ions/cm^2 at an energy of 90 keV. The layer 4 is bounded on the lower side by an n-type substrate 5.

It should be noted that the p-type layer 4 and the n-type substrate 5 are not essential to the invention. The layer 3 may be provided instead, for example, on an isolating substrate.

A sequence of transport electrodes 6, 7, 8 are provided on the surface above the semiconductor layer 3, which transport electrodes are constituted by conducting strips of, for example, metal or doped semiconductor material, such as polycrystalline silicon, and are separated by a blocking layer 9 from the layer 3. The blocking layer 9 is constituted in this embodiment by an isolating layer of silicon oxide. However, instead, if desired, a metal-semiconductor junction (Schottky junction) or a layer of another isolating material, such as, for example, silicon nitride, could also be used as a blocking layer.

The transport electrodes 6, 7, 8 are connected via clock lines $\phi1$, $\phi2$ and $\phi3$ to the clock voltage source 10. Fig. 3 indicates by way of example how the clock voltages V1, V2 and V3 at the clock lines $\phi1$, $\phi2$ and $\phi3$ can vary as a function of the time t. By means of these clock voltages, as is known, a moving pattern of potential wells can be induced in the layer 3, which potential wells are mutually separated by potential barriers and serve for storing and transporting information-carrying charge packets.

The charge is introduced via an input stage I (see Fig. 1), which is separated from the transport section T and comprises a supply zone 11 for supplying majority charge carriers, so in this embodiment electrons, of which the charge packets are composed. The supply zone is constituted in this embodiment by a highly doped n-type zone 11. This zone 11 is connected to a voltage source 12, which supplies to the supply zone 11 an input signal, which must be converted into a charge packet.

The input stage I further comprises an input electrode 13 located between the supply zone 11 and the transport electrodes 6, 7, 8 and separated by the isolating layer 9 from the semiconductor surface 2. By means of a voltage V13 applied to the input electrode 13, a potential well can be induced in the semiconductor layer 3, from which a charge packet is formed corresponding to the value of the input signal at the supply zone 11.

In this embodiment, a further sampling electrode 14 is provided for sampling the input signal between the supply zone 11 and the input electrode 13, by which electrode the supply of electrons from the supply zone 11 to the input electrode 13 can be interrupted.

An input signal source 12 (see Fig. 1) is connected to the supply zone 11 for applying a voltage difference between the supply zone 11 and the input electrode 13, which voltage difference determines the value of a charge carrier packet, so in this case a packet of electrons, which flows from the supply zone 11 into the potential well under the input electrode 13.

Since in charge-coupled devices of this kind, in which the charge carrier transport takes place in the interior of the semiconductor layer 3, the capacitances between the electrodes and the charge storage sites generally vary with the quantity of stored charge, the input characteristic (value of the charge packet as a function of the value of the input signal) is generally non-linear. In the device described here, (switching) means 15 are therefore provided, by which a potential well can be obtained under the input electrode 13, whose minimum is located closer to the surface than in the potential wells induced under the transport electrodes so that the input capacitance is much less dependent upon the stored charge.

According to the invention, a dopant of the second (so in this case p) conductivity type is further introduced between the supply zone 11 and the transport electrodes (6, 7, 8) in such a manner that the net doping of the first (n) conductivity type in the part of the semiconductor layer 3 bounded by the dotted line 20 between the supply zone 11 and the transport electrodes 6, 7, 8 is lower than in the remaining part of the layer 3. In the present embodiment, this additional p-doping was obtained by a second implantation of boron ions down to a depth of 4.0 μm at a dose of 1.1 . 10^{12} ions/cm^2 at an energy of 90 keV.

Due to the fact that a potential well with a potential maximum near the surface 2 is formed under the input electrode 13, the charge packet introduced via the electrode 13 is taken up for the major part by the capacitance constituted by the isolating layer 9.

This effect is increased additionally by the

measure according to the invention. Due to the fact that in the device according to the invention the n-doping of the layer 3 is reduced under the input electrode 13, much less charge can be received therein than in the transport section T of the layer 3. As a result, practically the whole charge packet under the input electrode is taken up by the linear input capacitance of the isolating layer 9.

Fig. 2 shows diagrammatically in plan view the transport electrodes 6, 7, 8 and the electrodes 11', 13 and 14 of the input stage I. It can be seen therefrom that the width of the electrodes 11', 13 and 14 of the input stage is smaller than that of the transport electrodes 6, 7 and 8. Due to the fact that the charge transport capacity of the electrodes of the input stage, in which the charge is stored at least for the major part at the surface, is higher per unit of electrode width than that of the transport electrodes, in fact the width of the electrodes of the input stage is preferably chosen so that the transport capacity of the electrodes in the input section and in the transport section is practically the same.

The operation of the device will now be described more fully by way of example. The various dopings, voltages etc. are given only by way of example; within the scope of the invention, a person skilled in the art will choose for each practical case the parameters suitable for an optimal operation of the device.

As indicated in Fig. 1, the substrate 5 is connected to a voltage of, for example, + 15 V with respect to earth. Via the output zone 22, a direct voltage of, for example, 20 V is applied to the layer 3. At a voltage of 0 V of the transport electrodes 6, 7, 8 and the electrodes 13, 14 of the input section I, the layer 3 can be depleted throughout its thickness, at least under these electrodes.

As indicated in Fig. 3, the clock voltages V1, V2 and V3 vary between 0 and 10 V. When a transport electrode 6, 7 or 8 is connected to 10 V, a potential well is formed under this electrode, whose potential maximum is located at a comparatively great depth in the layer 3 and in which electrons can be stored. At a voltage of 0 V at the electrode, any stored electrons are transferred to an adjacent site of higher potential. Between two successive potential wells, a potential barrier is formed by the intermediate electrode, which mutually separates the potential wells.

The input electrode 13 is connected to the voltage source 15, which supplies a voltage V13 (see Fig. 3). This voltage V13 varies between a lowest level, which is practically equal to the lowest level of the clock voltages V1, V2, V3, and a highest level. The highest level of V13, at which charge is stored under the electrode 13, in this example 10 V, is situated so that it is higher than the voltage at the supply zone 11, which latter

voltage is higher than the lowest potential under the transport electrode 6.

According to the invention, moreover the doping of the layer 3 under the electrode 13 is considerably reduced so that in situ very little charge can be stored in the layer 3. As a result, the charge carriers stored in this potential well will practically all be accumulated in the capacitance between the layer 3 on the one hand and the electrode 13 on the other hand. As a result, the linearity between the input signal and the output current is considerably improved. In the embodiment described, this linearity was about 99% and thus was practically equal to that of so-called surface CCD's.

The boron implantations in this embodiment are chosen so that due to the difference in threshold voltage between the input electrode 13 and the transport electrodes 6, 7, 8 in the operating condition an electrical field is obtained in the transport direction, which favours the speed of operation of the device.

In this embodiment, during sampling of the input signal, a voltage V14 is applied in the time interval between t1 and t2 (see Fig. 3) by means of the voltage source 21, which voltage is equal to the voltage at the electrode 13 so that no potential thresholds are present between the supply zone 11 and the input electrode 13. At the instant t2, the voltage V14 falls to 0 V. As a result, the said connection is interrupted by the potential barrier under the sampling electrode 14.

At the instant t3, the voltage at the input electrode 13 falls to 0 V and a voltage V1 of 10 V is applied to the electrode 6. The charge packet under the electrode 13 is thus transported to the potential well formed under the electrode 6. In the manner usual for charge-coupled devices of the BCCD type, the said packet is transported further by means of the clock voltages V1, V2 and V3 via the bulk of the layer 3 to the output 22, at which the information is read out by means of a read-out member 27.

The invention is not limited to the embodiment described here. Within the scope of the invention defined in the Claims, many variations are possible for those skilled in the art.

For example, the various dopings not only may have different values, but their signs may also be inverted (simultaneously) with simultaneous reversal of the voltages applied. Further, the layers 3 and 4 may also be formed, for example, by diffusion or epitaxially instead of by ion implantation. Moreover, the introduction of the dopant of the second conductivity type according to the invention may take place, instead of by implantation, also in a different manner, for example by diffusion or by a combination of implantation and diffusion. Other embodiments of charge-coupled devices, in which

the invention may advantageously be used, are described, for example, in the aforementioned US PS 4280068, whose contents are considered as being incorporated in the present Application.

Claims

1. A charge-coupled device having a semiconductor body comprising a semiconductor layer of a first conductivity type adjoining a surface, means for depleting the semiconductor layer throughout its thickness at least in the absence of supply of majority charge carriers whilst avoiding breakdown, a sequence of transport electrodes on the surface above the semiconductor layer, which are separated from this layer by a blocking layer and are connected to clock voltage sources to form in the semiconductor layer potential wells separated from the surface for storing and transporting information-carrying charge packets, an input stage comprising a supply zone for supplying said majority charge carriers and an input electrode, which is located between the supply zone and the transport electrodes, is separated from the semiconductor surface by an isolating layer and by which in the semiconductor layer a potential well can be induced with an input signal source for applying a voltage difference between the supply zone and the input electrode, which determines the value of a charge carrier packet flowing from the supply zone into the potential well under the input electrode, while in order to obtain a practically linear relation between the value of the said charge carrier packet, and the input signal, means are provided, by which a potential well can be obtained under the input electrode, whose minimum is located closer to the surface than in the potential wells induced under the transport electrodes, characterized in that a dopant of the second opposite conductivity type is introduced between the supply zone and the transport electrodes in such a manner that the net doping of the first conductivity type in the part of the semiconductor layer between the supply zone and the transport electrodes is lower than in the remaining part of the layer.

2. A charge-coupled device as claimed in Claim 1, characterized in that the width of the electrodes of the input stage is chosen so that the transport capacity of these electrodes is practically equal to that of the transport electrodes.

3. A charge-coupled device as claimed in Claim 1 or 2, characterized in that the net doping of the

semiconductor layer under the input electrode
is chosen so that due to the difference in
threshold voltage between the input electrode
and the transport electrodes in the operating
condition an additional electrical field is ob-   5
tained in the transport direction.

4. A charge-coupled device as claimed in any
one of the preceding Claims, characterized in
that a sampling electrode is provided between   10
the supply zone and the input electrode for
sampling the input signal, which electrode is
provided with means by which during sampling
a potential can be applied in the semiconduc-
tor layer, as a result of which the supply of   15
majority charge carriers from the supply zone
to the input electrode can be blocked.

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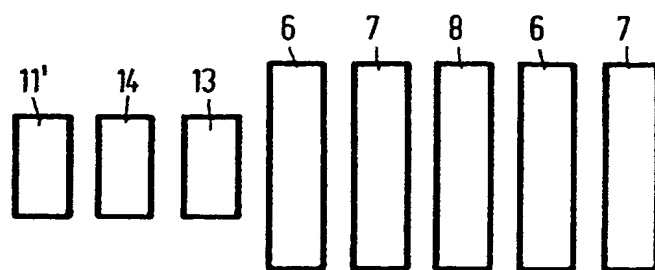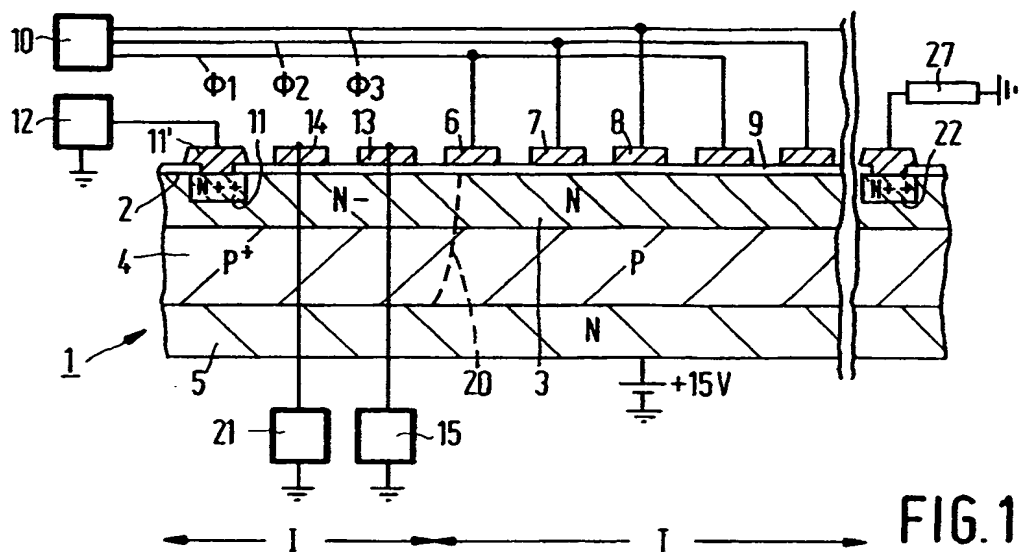30

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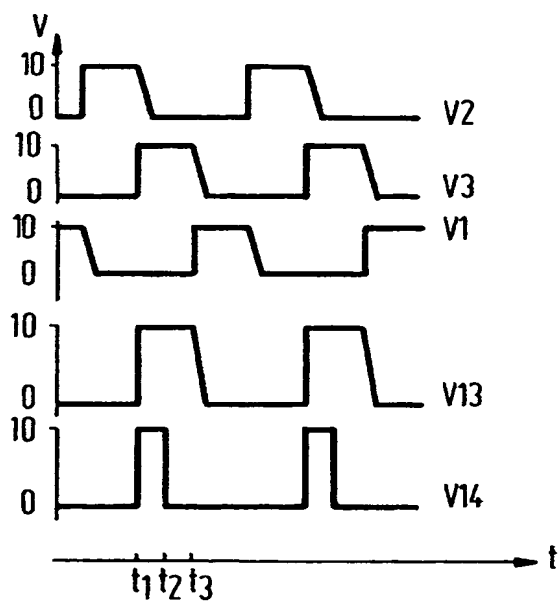
FIG.1

FIG.2

FIG.3

EUROPEAN SEARCH
REPORT

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	FR-A-2 399 773 (RCA CORP.) * Page 1, line 33 - page 2, line 30; figures 1,2 * – – –	1,2	H 01 L 29/796
A	EP-A-0 205 221 (N.V. PHILIPS' GLOEILAMPEN-FABRIEKEN) * Column 3, line 8 - column 4, line 39; figures 1,2 * – – –	1,2	
A	EP-A-0 001 146 (N.V. PHILIPS' GLOEILAMPEN-FABRIEKEN) * Abstract; figure 1 * US-A-4 280 068 (Cat. D,A) – – – – –	1	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)
H 01 L

The present search report has been drawn up for all claims

Place of search	Date of completion of search	Examiner
The Hague	07 May 91	BAILLET B.J.R.